In the claims:

Please amend claims 1-2 and 4-6. The claims are as follows.

1. (Currently amended) A semiconductor structure, comprising:

first and second source/drain regions, wherein the first and second source/drain regions each comprise dopants of a first doping polarity;

a semiconductor channel region disposed between the first and second source/drain regions;

a semiconductor buried well region in direct physical contact with the semiconductor channel region, wherein the semiconductor buried well region comprises dopants of a second doping polarity opposite to the first doping polarity; and

a buried barrier region being disposed between the semiconductor buried well region and the first source/drain region and being disposed between the semiconductor buried well region and the second source/drain region,

wherein the buried barrier region is adapted for preventing leakage current between the semiconductor buried well region and the first source/drain region and between the semiconductor buried well region and the second source/drain region.

2. (Currently amended) The semiconductor structure of claim 1, further comprising:

a gate region; and

a gate dielectric layer disposed between and electrically insulating the gate region and the semiconductor channel region from each other,

wherein the semiconductor channel region is sandwiched between the gate dielectric layer and the semiconductor buried well region.

3. (Original) The semiconductor structure of claim 2, wherein the gate region comprises polysilicon.

4. (Currently amended) The semiconductor structure of claim 1,

wherein the semiconductor channel region and the semiconductor buried well region share a common interfacing surface that defines a reference direction perpendicular to the a common interfacing surface and pointing from the semiconductor buried well region to the semiconductor channel region, and

wherein a portion of the first source/drain region is farther away from the common interfacing surface in the reference direction than the entire semiconductor channel region.

~~wherein the buried barrier region comprises silicon dioxide.~~

5. (Currently amended) The semiconductor structure of claim 4, wherein a portion of the second source/drain region is farther away from the common interfacing surface in the reference direction than the entire semiconductor channel region.~~claim 1, wherein the first and second source/drain regions are heavily doped.~~

6. (Currently amended) The semiconductor structure of claim 1, further comprising an underlying dielectric layer, wherein the first and second source/drain regions are on top of and in direct physical contact with the underlying dielectric layer. ~~wherein the buried well region is heavily doped.~~

7. (Withdrawn) A method for forming a semiconductor structure, the method comprising the steps of:

(a) providing a semiconductor substrate covered on top with a mandrel layer;

(b) etching a trench through the mandrel layer and into the substrate;

(c) forming a buried barrier region on a side wall of the trench, wherein the buried barrier region is in direct physical contact with both the substrate and the mandrel layer;

(d) forming a buried well region and a channel region in the trench, wherein the channel region is on top of the buried well region; and

(e) forming first and second source/drain regions,

wherein the channel region is disposed between the first and second source/drain regions, and

wherein the buried barrier region is disposed between the buried well region and the first source/drain region and is disposed between the buried well region and the second source/drain region.

8. (Withdrawn) The method of claim 7, wherein the buried well region is heavily doped.

9. (Withdrawn) The method of claim 7, wherein the buried barrier region is adapted for essentially eliminating junction capacitance (i) between the buried well region and the first source/drain region and (ii) between the buried well region and the second source/drain region.

10. (Withdrawn) The method of claim 7, wherein the buried barrier region is adapted for essentially eliminating leakage current (i) between the buried well region and the first source/drain region and (ii) between the buried well region and the second source/drain region.

11. (Withdrawn) The method of claim 7, wherein the step of forming the buried barrier region comprises the steps of:

depositing a buried barrier layer on side and bottom walls of the trench such that the buried barrier layer is in direct physical contact with both the substrate and the mandrel layer; and

etching away a portion of the buried barrier layer at the bottom wall of the trench so as to form the buried barrier region from the buried barrier layer.

12. (Withdrawn) The method of claim 7, wherein the buried barrier region comprises silicon dioxide.

13. (Withdrawn) The method of claim 7, wherein the step of forming the buried well region and the channel region comprises the steps of:

depositing a semiconductor material in the trench so as to form an under-gate region such that the buried barrier region is completely buried in the under-gate region; and

doping a portion of the under-gate region which is surrounded by the buried barrier region,

wherein the doped portion of the under-gate region comprises the buried well region, and

wherein an undoped portion of the under-gate region on top of the buried well region comprises the channel region.

14. (Withdrawn) The method of claim 13, wherein the semiconductor material is deposited in the trench by growing silicon epitaxially.

15. (Withdrawn) The method of claim 13, wherein the doped portion of the under-gate region is doped by ion implantation.

16. (Withdrawn) The method of claim 7, further comprising the steps of:

forming a gate dielectric layer on top of the channel region; and then

forming a gate region on top of the gate dielectric layer before the step of forming first and second source/drain regions,

wherein the gate region is electrically insulated from the channel region by the gate dielectric layer.

17. (Withdrawn) A method for forming a semiconductor structure, the method comprising the steps of:

(a) providing a semiconductor substrate covered on top with a mandrel layer;

(b) etching a trench through the mandrel layer and into the substrate;

(c) forming a buried barrier region on a side wall of the trench, wherein the buried barrier region is in direct physical contact with both the substrate and the mandrel layer;

(d) depositing a semiconductor material in the trench so as to form an under-gate region such that the buried barrier region is completely buried in the under-gate region;

(e) forming a gate spacer region on side walls of the trench;

(f) doping via the trench a portion of the under-gate region which is surrounded by the buried barrier region, wherein the doped portion of the under-gate region comprises a buried well region, and wherein an undoped portion of the under-gate region on top of the buried well region comprises a channel region;

(g) forming a gate dielectric layer on top of the channel region;

(h) forming a gate region on top of the gate dielectric layer, wherein the gate region is electrically insulated from the channel region by the gate dielectric layer; and

(i) forming first and second source/drain regions in the substrate,

wherein the channel region is disposed between the first and second source/drain regions,

wherein the buried barrier region is disposed between the buried well region and the first source/drain region and is disposed between the buried well region and the second source/drain region, and

wherein the buried barrier region is adapted for preventing leakage current between the buried well region and the first source/drain region and between the buried well region and the second source/drain region.

18. (Withdrawn) The method of claim 17, wherein the step of forming the buried barrier region comprises the steps of:

depositing a buried barrier layer on side and bottom walls of the trench such that the buried barrier layer is in direct physical contact with both the substrate and the mandrel layer; and

etching away a portion of the buried barrier layer at the bottom wall of the trench so as to form the buried barrier region from the buried barrier layer.

19. (Withdrawn) The method of claim 18, wherein the buried barrier layer comprises silicon dioxide.

20. (Withdrawn) The method of claim 17, wherein the step of forming the gate spacer region comprises the steps of:

forming a gate spacer layer on side and bottom walls of the trench; and

removing a portion of the gate spacer layer on the bottom wall of the trench so as to form the gate spacer region from the gate spacer layer.

21. (Withdrawn) A method for forming a semiconductor structure, the method comprising the steps of:

(a) providing a silicon-on-insulator (SOI) substrate covered on top with a mandrel layer, wherein the SOI substrate includes (i) an upper semiconductor layer, (ii) a lower semiconductor layer, and (iii) an electrical insulator layer sandwiched between the upper and lower semiconductor layers;

(b) etching a trench through the mandrel layer and into the SOI substrate such that the lower semiconductor layer is exposed to the atmosphere at a bottom wall of the trench;

(c) forming a buried barrier region on a side wall of the trench, wherein the buried barrier region is in direct physical contact with both the SOI substrate and the mandrel layer;

(d) forming a buried well region and a channel region in the trench, wherein the channel region is on top of the buried well region; and

(e) forming first and second source/drain regions,

wherein the channel region is disposed between the first and second source/drain regions, wherein the buried barrier region is disposed between the buried well region and the first source/drain region and is disposed between the buried well region and the second source/drain region.

22. (Withdrawn) The method of claim 21, wherein the buried well region is heavily doped.

23. (Withdrawn) The method of claim 21, wherein the buried barrier region is adapted for essentially eliminating junction capacitance (i) between the buried well region and the first source/drain region and (ii) between the buried well region and the second source/drain region.

24. (Withdrawn) The method of claim 21, wherein the buried barrier region is adapted for essentially eliminating leakage current (i) between the buried well region and the first source/drain region and (ii) between the buried well region and the second source/drain region.

25. (Withdrawn) The method of claim 21, wherein the step of forming the buried barrier region comprises the steps of:

depositing a buried barrier layer on side and bottom walls of the trench such that the buried barrier layer is in direct physical contact with both the substrate and the mandrel layer; and

etching away a portion of the buried barrier layer at the bottom wall of the trench so as to form the buried barrier region from the buried barrier layer.

26. (Withdrawn) The method of claim 21, wherein the buried barrier region comprises silicon dioxide.

27. (Withdrawn) The method of claim 21, wherein the step of forming the buried well region and the channel region comprises the steps of:

depositing a semiconductor material in the trench so as to form an under-gate region such that the buried barrier region is completely buried in the under-gate region; and

doping a portion of the under-gate region which is surrounded by the buried barrier region,

wherein the doped portion of the under-gate region comprises the buried well region, and

wherein an undoped portion of the under-gate region on top of the buried well region comprises the channel region.

28. (Withdrawn) The method of claim 27, wherein the semiconductor material is deposited in the trench by growing silicon epitaxially.

29. (Withdrawn) The method of claim 27, wherein the doped portion of the under-gate region is doped by ion implantation.

30. (Withdrawn) The method of claim 21, further comprising the steps of:

forming a gate dielectric layer on top of the channel region; and then

forming a gate region on top of the gate dielectric layer before the step of forming first and second source/drain regions,

wherein the gate region is electrically insulated from the channel region by the gate dielectric layer.